ABSTRACT

A method of fabricating an SMOS integrated circuit with source and drain junctions utilizes an offset gate spacer for N-type transistors. Ions are implanted to form the source and drain regions in a strained layer. The offset spacer reduces problems associated with Arsenic (As) diffusion on strained semiconductor layers. The process can be utilized for SMOS metal oxide semiconductor field effect transistors (MOSFETs). The strained layer can be a strained silicon layer formed above a germanium layer.